Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to further clarify Applicants disclosed and claimed invention.

Support for the amendments is found in the previously presented claims

No new matter has been added.

For example support for the amendments is found in the previously presented claims and in the Specification at paragraph 0053:

"As shown in Figure 3G, a second (top) dielectric layer 50 is deposited over the assembly shown in Figure 3F to provide a substantially planar surface overlying the electrically redistribution traces 48. The second dielectric layer 50 may be made of any suitable material known to those skilled in the art, including spin-on polyimide or BCB. As shown in Figure 3E, a second set of vias 52 are formed in the second dielectric layer 50 wherein each via 52 is aligned with an associated redistribution trace 48. The second set of vias 52 may be formed by standard photoresist patternization and etching techniques known to those skilled in the art. Thereafter, electrically conductive bumps 54, for example, solder, gold, silver, nickel, tin containing bumps, are formed on the assembly with each solder bond extending through the vias 52 formed in the second

dielectric layer 50 and makes electrical connection to the redistribution trace 48. Additional metallization layers may be interposed between the electrically conductive bump 54 and the redistribution trace 48. The electrically conductive bump 54 may be formed by any manner formed to those skilled in the art, including, for example but not limited to, placing balls over the vias 52, stenciling, or plating **and subsequent reflow.**"

Claim Rejections under 35 USC 112

Claims 42-44 have been amended to overcome Examiners rejections.

Claim Rejections under 35 USC 103

1. Claims 1-8, 11, 14, 16, 18-22, 25, 28, 30, 32-36, 38, and 41, stand rejected under 35 USC 103(a) as being unpatentable over Chen et al. (US 7.087,991), in view of Chua et al. (6,825,553), in further view of Honda (US 7,074,650).

Chua et al. disclose forming **cavities (by anisotropic etching) in a silicon substrate** where the cavities are about the size of an individual dies and the bottom of the cavities is coated with a **die attach material (adhesive) (including polyimide**

or BCB) (item 218, Figure 2B; col 7, lines 15-35). **An undisclosed type of dielectric layer is then formed over the die in the cavities** by spin or spray coating including filling gaps between the substrate and die. Vias are then formed to expose bond pads on the dies and a metallization layer (redistribution layer) is formed on the dielectric layer to connect to the bond pads through the vias (col 7, lines 38-65). Chua et al. disclose that the metallization layer may be **formed of aluminum or copper "or other metals known in the art"** (col 8, lines 1-10) and that the bond pads may be treated with undisclosed underbump metallization prior to forming the metallization layer to improve adhesion.

Chua et al. also teach forming vias in an uppermost **dielectric layer (undisclosed type)** (over metallization layers) where **solder balls** or other conductive bumps are formed **within the openings** to connect to the underlying metallization layers (col 4, lines 65-68; col 8, lines 31-39; item 320, Figure 3F).

Thus, Chua et al. fail to teach several aspects of Applicants disclosed and claimed invention including Applicants first and second dielectric layers. As noted above, Chua et al.

teach using **polyimide or BCB) as the adhesive material** to attached the chip within the cavities.

On the other hand, Chen et al. teach that a first insulating layer (first dielectric layer) (320 Figure 3G; 320-1; Figure 6) is a photo-imageable material, glass, resin or other cured material (col 4, lines 1-7). Chen et al. also teach forming a "passivation layer (also 320; Figure 3H; 320-2 Figure 6) such as a solder mask" (col 4, lines 46-51) over a patterned circuit layer, prior to patterning the passivation layer **to attach solder** balls to solder ball pads (**"solder balls are planted onto solder ball pads"** - col 4, lines 52-54; col 3, lines 1-3; col 6, lines 16-17), where the solder ball pads (346; Fig 3I, Fig 6) are formed on portions of the patterned circuit layer by patterning the passivation layer (col 4, lines 46-51).

Chen et al. appear to disclose that pre-formed solder balls are attached to solder ball pads through the passivation layer by something other than a solder reflow process.

Chen et al. further teach that the chip may be bonded to the substrate by a conductive bonding paste or a non-conductive bonding material such as adhesive tape (col 3, lines 60-67).

Chen et al. further teach that the substrate can be a metallic layer, a glass layer, or a polymer material layer (col 5, lines 38-42). However, Chen et al. teach that in an important aspect of the invention the IC package has a higher heat dissipation (col 2, lines 45-46;) and that a **metallic or thermally conductive substrate is preferred** (col 5, lines 38-43; col 6, lines 56-64) col 5 and further, that the substrate may **include an internal circuit** (col 5, lines 44-54) which is **connected to bond pads on the substrate (outside of the cavity)** (see 316, Figure 6; claim 1). Alternately, the package can be **formed with no cavity** (Fig 7).

Nowhere do Chua et al. disclose or suggest "forming a first dielectric layer over the first surface of the chip carrier substrate and over the integrated circuit chip in each of the cavities wherein the first dielectric layer comprises at least one of a polyimide and BCB."

On the other hand, Honda discloses a significantly different structure where upward protruding pad/post electrodes (15; Fig 12A) are formed on a wiring pattern (11) and solder bumps (16) are formed on the post electrodes (15) by mounting a solder ball on fluxed post electrodes and subjecting to heating reflow to form a solder bump (16), followed by washing the solder bump to remove the flux (col 8, lines 58-64)and then mounting a support plate with preformed holes larger than the solder bumps around the solder bumps (17; Figure 12B) supported on height adjustment jigs (19) followed by injecting an insulating resin (disclosed to be polyimide) around the post electrodes and solder bumps (20; see Figure 13; col 8, lines 65- col 9, line 15).

There is not apparent motivation for combining the thermosetting injected resin injected underneath a support plate to surround a post electrode an a portion of the solder bump with the methods or structures of either Chua et al. or Chen et al. For example, using the injected thermosetting resin of Honda (with support plate) to form the passivation layer of Chen et al. would change the principle of operation of Chen et al. which is to pattern the passivation layer prior to attaching/planting solder balls, and the support plate would make the device of Chen et al. unsuitable for its intended purpose.

Nevertheless, even assuming arguendo, a proper motivation for combining the teachings of Honda with either Chen et al. or Chua et al., such combination would not produce Applicants invention including in claims 1 and 20:

"forming **a second dielectric layer comprising at least one of a polyimide and BCB over the redistribution traces, and forming a second set of vias in the second dielectric layer** so that each of the second set of vias communicates with one of the redistribution traces; and,

forming electrically conductive bumps by reflow wherein each electrically conductive bump overlies the second dielectric layer and comprises an unrounded portion extending into one of the vias formed in the second dielectric layer and so that the electrically conductive bump is electrically connected to one of the redistribution traces."

Or as in claim 34:

"a second dielectric layer over the redistribution traces,

and **a second set of vias in the second dielectric layer so that each of the second set of vias communicates with one of the redistribution traces, wherein the second dielectric layer comprises at least one of a polyimide and BCB;**

electrically conductive bumps wherein **each electrically conductive bump overlies the second dielectric layer and comprises an unrounded portion extending into one of the vias formed in the second dielectric layer** and so that the electrically conductive bump is electrically connected to one of the redistribution traces."

Moreover, none of the cited references discloses or suggests as in claim 20 wherein "said semiconductor chip carrier substrate selected from the group consisting of **silicone and plastic;**"

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Examiner argues that using polymides as the second dielectric layer is a matter of design choice since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use, citing In re Leshin, 125 USPQ 416.

However, Examiner has not shown in the prior art a recognition of suitability for intended use in the structures of either Chen et al. or Chua et al., and nevertheless the combination of teachings would not produce Applicants invention.

A statement that modifications of the prior art to meet the claimed invention would have been "'well within the ordinary skill of the art at the time the claimed invention was made'" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).*

2. Claims 15, 29, and 40 stand rejected under 35 USC 103(a) as being unpatentable over Chen et al. in view of Chua et al., in

further view of Honda, and in further view of Becker et al (6,617,674).

Applicants reiterate the comments made above with respect to Chen et al., Chua et al., and Honda.

Even assuming *arguendo* that Becker is analogous art and a proper motivation for combination, the fact that Becker et al. disclose forming a package by forming an overlying layer of silicone except for covering bonding pads and forming metal traces with one end on the bond pad and on the surface of the silicone where the metal trace is titanium/nickel/copper and a solder ball is at the distal end of the trace, does not further help Examiner in producing Applicants invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

3. Claims 9, 10, 23, and 24 stand rejected under 35 USC 103(a) as being unpatentable over Chen et al. in view of Chua et al., in further view of Honda, and in further view of Benavides et al. (6,548,895).

Applicants reiterate the comments made above with respect to Chen et al., Chua et al., and Honda.

Even assuming *arguendo* that Benavides et al. is *analogous* art and a proper motivation for combination, that fact that Benavides et al. disclose forming **fluidic channels (trenches) in a substrate for an electro-microfluidic by a variety of material removal methods** such as "milling with a miniature milling tool, laser milling, chemical etching, or abrasive jet spray milling" **or alternatively, that parts of the microfluid device on the substrate can be fabricated by using additive processes**, such as "rapid prototyping with built-up plastic layers, thermal spray metal deposition, cold spray deposition, Laser Engineered Net Shape (LENS.TM.) directed metal deposition, casting, **molding**, injection molding of a moldable material, cold-isostatic processing, hot isostatic processing, sintering, lamination, etc.", does not further help Examiner in producing Applicants disclosed and claimed invention.

Moreover, Examiner has not shown in the prior art that etching, molding and milling are known equivalents.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

4. Claims 12, 17, 26, and 31 (apparently) stand rejected under 35 USC 103(a) as being unpatentable over Chua et al., above, in view of Volfson et al. (US 5,106,461).

Applicants reiterate the comments made above with respect to Chen et al., Chua et al., and Honda.

Assuming *arguendo* a proper motivation for combination, the fact that Volfson et al. disclose reactive ion etching to form vias in a dielectric layer does not further help Examiner in producing Applicants invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed: Cir. 1991).*

Conclusion

The cited references, alone or in combination, fail to produce Applicants disclosed and claimed invention and therefore fail to make out a *prima facie* case of obviousness with respect to Applicants independent and dependent claims.

Applicants have further amended the claims to further clarify their disclosed and claimed invention and respectfully request favorable reconsideration by Examiner.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in

condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

Tung & Associates

Randy W. Tung
Reg. No. 31,311
Telephone: (248) 540-4040